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(54) Trenched DMOS transistor fabrication using seven masks

(57) A trenched DMOS transistor is fabricated using seven masking steps. One masking step defines both the P+ deep body regions and the active portions of the transistor which are masked using a LOCOS process. A second masking step defines the insulating oxide in the termination region. The insulating (oxide) layer in the termination region is thus thicker than in the active region of the transistor, thereby improving process control and reducing substrate contamination during processing. Additionally, the thicker field oxide in the termination region improves electric field distribution so that avalanche breakdown occurs in the cell (active) region rather than in the termination region, and thus breakdown voltage behavior is more stable and predictable.

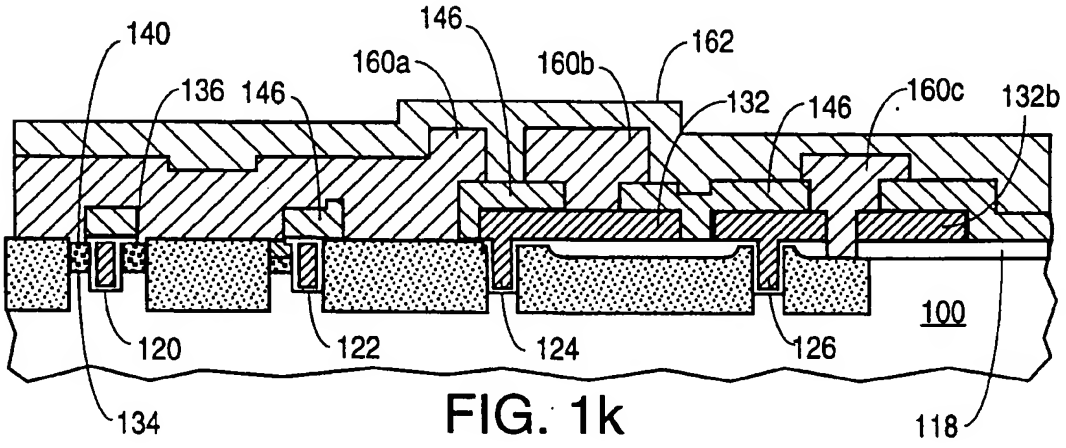

FIG. 1k

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Description

This application is related to commonly owned U.S. Patent No. 5,316,959, entitled "Trenched DMOS Transistor Fabrication Using Six Masks", issued May 31, 1994.

This invention relates to a method for fabricating a trenched DMOS transistor using e.g. seven masking steps, resulting in a transistor having narrow trenches, shallow diffusions, and formed using relatively few process steps, and having a thick dielectric layer in the termination region.

DMOS transistors are well known as a type of MOSFET (metal on semiconductor field effect transistor) using diffusions to form the transistor regions, with a typical application being as a power transistor. Such devices enjoy widespread use in such applications as automobile electrical systems, power supplies, and power management applications.

Many different processes have been used for the fabrication of power MOSFET devices over the years; these are generally deep diffusion processes. It is also well known to form such transistors having a trench in the substrate, the trench being lined with a thin oxide layer and filled with a conductive polysilicon to form the transistor gate structure.

Prior art trenched DMOS transistors have the shortcoming that typically it takes a fairly large number (such as eight or nine) fabrication masking steps to define the various transistor regions, including the tubs in which the active transistor regions are formed, the body region of the transistor, the source region of the transistor, the body contact regions, each of which are separate diffusions, and the termination structures, i.e. field plates and field rings. Additional masking steps define the oxide layers and polysilicon portions of the transistor. Each additional masking step requires a mask alignment and thus results in the possibility of alignment error, undesirably reducing yield. Additionally, the many process steps which include temperature cycles tend to result in unwanted diffusion of certain of the implanted ions, thus undesirably altering the lateral extent and/or depth of various of the diffused regions.

Thus there is a need for transistor fabrication processes using relatively few masks.

The process and resulting transistor structure of the above-referenced patent provide the same oxide (dielectric) layer thickness in the active (gate) region of the transistor as in the termination (edge) portion of the transistor. This has been found to be somewhat disadvantageous because breakdown instability is observed probably due to the charging effect from the passivation layer and floating gate.

In accordance with the invention, a trenched DMOS transistor has relatively narrow and shallow trenches in one embodiment with relatively shallow associated transistor active regions. By using an additional masking step to expose the principle surface of the substrate in the termination region of the transistor prior to growing the thick field oxide, a field oxide dielectric layer is provided in the termination region which is relatively thicker than the gate oxide in the active portions of the transistor. Advantageously the thicker field oxide in the termination region improves electric field distribution so that avalanche breakdown occurs in the cell (active) region rather than in the termination region, and thus breakdown voltage behavior is more stable and predictable. Furthermore, process control is improved due to this thicker oxide. Additionally, thicker oxide in the termination region prevents dopant or ionic contamination of the underlying substrate from the overlying layers, thereby reducing leakage current problems in the termination region.

In one embodiment, in addition to the thick field oxide in the termination region, also present in the termination region is a field plate which is electrically connected to a guard ring by a metallized contact and shorted to the source region in the transistor active region.

Figures 1a through 1k show in cross section a sequence of steps to form a transistor in accordance with the present invention.

The present invention is to be understood in the context of two commonly owned other disclosures, both incorporated herein by reference. The first of these is U.S. Patent No. 5,304,831, entitled "Low On-Resistance Power MOS Technology", inventors Hamza Yilmaz et al., which discloses a method for fabricating a DMOS transistor using five masking steps. The second is U.S. Patent Application Serial No. 07/918,996, filed July 23, 1993 entitled "Field Effect Transistor Having Edge Termination Utilizing Trench Technology", inventor Izak Bencuya, attorney docket number M-2140.

A process in accordance with the invention and using seven masking steps is described hereinafter. It is to be understood that the reference herein to "seven masking masking steps" is illustrative and not limiting; other processes with other numbers of masking steps are also in accordance with the present invention.

In Figure 1a an N-channel process in accordance with the invention uses an N- doped epitaxial layer 100 having a resistivity of for example 0.20 to 2.0 ohm-cm formed on a conventional N+ doped silicon substrate (not shown), the layer 100 having a resistivity of for example 0.001 to 0.010 ohm-cm and being 5 to 15 microns (micrometers) thick. The substrate is about 500 μm thick. A thin layer of silicon dioxide 102 is thermally grown 300Å to 500Å thick on the principal surface of the epitaxial layer 100, and a mask layer of silicon nitride 104 having a thickness of from 100Å to 2000Å is deposited thereon. Mask layer 104 is conventionally patterned and etched. Then boron is predeposited by using the boron nitride process or by implanting boron at an energy of 30 to 60 KeV and a dose of 2×10^{13} to $1 \times 10^{16}/cm^2$ through the mask layer 104 and driven in to form P+ deep body regions 106, 108 which are about 2 to 3 microns deep and having a final concentration at the principal surface of 1×10^{16} to $2 \times 10^{19}/cm^3$, and similar p+ field rings (termi-

nation structures) 110, 112, 114.

Then in Figure Ib, an additional mask is used to pattern mask layer 104 in the termination region 116, exposing the relatively thin gate oxide layer 102. This additional masking step is an improvement herein over the method disclosed in the above referenced Patent No. 5,316,959.

Then local oxidation (LOCOS) 118 of silicon to a thickness of 5,000 to 8,000Å in Figure Ic to grow the thicker field oxide layer is followed by stripping of the nitride mask layer 104 to define both the active transistor cells and the device termination portion. (It is to be understood that in Figures 1a to 1k, the device termination region is located at the right hand side of the figures and the central active cell portion of the transistor is at the left hand portion of the figures. Also, the process steps are shown schematically and not to scale.)

As shown in Figure Ic, thick field oxide layer 118 extends over termination region 116.

Then in Figure 1d an LTO (low temperature oxide) second mask layer (not shown) is conventionally deposited and patterned, and trenches 120, 122, 124, 126 are each formed by anisotropic reactive ion dry etching to a depth of 1.5 to 3 microns and a width of 1 to 2 microns. Trenches 120, 122, 124 serve as the gate electrode trenches and trenches 124, 126 separate the field rings from adjacent structures. After the trench walls and corners are smoothed by an isotropic plasma "round hole" etch and a sacrificial oxide growth and subsequent stripping of the sacrificial oxide, the gate oxide layer 130 is conventionally grown on the sidewalls of the trenches 120, 122, ..., 126 to a thickness of 100 to 1000Å.

Then in Figure Ie the trenches are planarized by the deposition of a layer of polycrystalline silicon 132 which is at least as thick as the width of each trench. This relatively thick polysilicon layer 132 is partially dry etched away (without a mask) leaving a thickness of 0.5 microns. By protecting the principal surface with photo resist (not shown), the substrate back side polysilicon and oxide layers are removed by wet chemical etch. The remaining polysilicon 132 is then doped to a conductivity less than 2 ohm/square. Then masking of polysilicon 132 and a second polysilicon "defreckable" etching is performed, resulting in the structure of Figure Ie defining windows for subsequent processing. The use of the LOCOS oxide process eliminates the prior art "poly stringer" problem by reducing the oxide step height.

This is followed in Figure If by a blanket boron P-body implant and diffusion at an energy of about 60 KeV and dose of 2×101^3 to $5 \times 10^{13}/cm^2$ providing a final surface concentration of about $2 \times 10^{17}/cm^3$ forming body regions 134, 136, 138.

Then a blanket N+ arsenic source implant and diffusion are performed at an energy of 60 to 120 KeV at a dosage of 1×10^{15} to $1 \times 10^{16}/cm^2$ to achieve a final surface concentration of $5 \times 10^{19}/cm^3$ in Figure 1g forming N+ source regions 140, 142. The N+ source regions 140, 142 depth is about 0.5 microns.

Then in Figure 1h a layer of boro-phosphorsilicate glass (BPSG) 146 is conventionally deposited to a thickness of about 1.35 microns over the entire structure. Then in Figure Ii BPSG layer 146 is masked and patterned to define the electrical contact openings 150, 152, 154, 156 to the transistor structure. Also, opening 158 in the termination region BPSG layer 146 is formed in this step. The BPSG layer 140 is then conventionally reflowed to smooth its corners.

Then in Figure 1j a layer of metal 160 (e.g. aluminum or aluminum plus 1% silicon) is deposited over the entire structure, such as by sputtering and then etched using a conventional patterned mask layer.

Then in Figure 1k a passivation layer 162 such as PSG or plasma nitride is conventionally deposited and by a mask step, bonding pad openings (not shown) to contact the gate and source area are opened therethrough.

In contrast to the final structure disclosed in the above-referenced U.S. Patent No. 5,316,959, here the thick field oxide layer 118 extends to the edge of the termination region at the right side of Figure 1k, providing the above-described benefits. Also, here the P+ doped region 114 is contacted by overlying metal contact 160c. The resulting termination structure is a P+ guard ring 114 electrically connected to polysilicon plate 132b via contact 160c and to the transistor source regions.

The polysilicon field plate 132b improves breakdown voltage in the termination region by smoothing the electric field distribution near the P+/N junction in the termination region.

As will be recognized, seven masking steps are thereby utilized in one embodiment of the fabrication process described in Figures 1a to 1j of the present invention. These seven masking steps are as follows:

1) a deep body P+ masking step in which openings are formed in layer 102 as shown in Figure 1a through which P+ regions are doped;

2) a termination region mask patterning step in which an additional opening is formed in mask layer 104 for growing LOCOS oxide layer 118 over the termination region 116 shown in Figure 1b;

3) a trench masking step in which a layer of photoresist is patterned to define the trenches 120, ..., 126 shown in Figure 1d;

4) a polysilicon masking step in which a layer of photoresist is used to protect and thereby to define the portions of polysilicon layer 132 shown in Figure 1e;

5) a contact opening masking step in which portions of a BPSG layer 146 are removed to define a contact to the P+ regions and to define a contact to the doped polysilicon in trench 124 of Figure 1i.

6) a metal masking step in which portions of a metal

layer 160 are removed to define the metal source electrode 160(a), the metal gate finger 160(b), and the guard ring contact 160c of Figure 1j; and

7) a conventional pad masking step in which portions of passivation layer 162 are removed to expose a gate bonding pad and source bonding pad.

It is to be understood that the above-described process is for fabricating an N-channel vertical DMOS transistor device as shown. By reversal of the various semiconductor region doping types the opposite type, a P-channel vertical DMOS transistor structure may also be formed.

With reference to the structure of Figure 1k, the field rings 112, 114 are separated by insulated trench 126, thus allowing the field rings to be closely spaced together and hence conserving chip surface area. Trench 126 is filled with doped polysilicon. Trench 124 is also filled with polysilicon and is electrically connected to the gate finger electrode connected in turn (outside the plane of Fig. 1j) to the doped polysilicon which fills trenches 120, 122. The drain electrode is conventionally formed on the back side (not shown) of the substrate.

The area immediately to the right of trench 122 has no active (source or body) regions and hence serves as a dummy cell adjacent to the termination structures; this dummy cell can be dispensed with in one embodiment. Also, the above described process can be implemented in a transistor having a termination other than that described herein.

The above description is illustrative and not limiting; further modifications will be apparent to one skilled in the art in light of this specification and are intended to fall within the scope of the appended claims.

Claims

1. A method for forming a field effect transistor comprising:

providing a semiconductor substrate having a principal surface and being of a first conductivity type;

forming a patterned mask layer on the principal surface;

doping semiconductor regions of a second conductivity type in portions of the substrate exposed by the mask layer, thereby forming deep body regions of the transistor;

growing an oxide layer on portions of the principal surface exposed by the mask layer including on a portion of a termination region of the transistor;

forming a plurality of trenches in the substrate;

forming a layer of conductive material in the trenches and over at least a part of the oxide layer, the portion of the conductive material layer in the trenches being a gate of the transistor;

forming doped first regions of the second conductivity type in the substrate extending from the unmasked portions of the principal surface into the substrate;

forming doped second regions of the first conductivity type extending from the unmasked portions of the principal surface into the substrate, the first and second doped regions respectively being body and source regions of the transistor;

forming a patterned insulating layer overlying the principal surface and the conductive material layer; and

forming a patterned interconnect layer overlying the principal surface and over the patterned insulating layer and contacting the deep body, body, and source regions, and the gate electrode.

2. The method of Claim 1, wherein the step of forming a layer of conductive material comprises forming a portion of the conductive material layer in the termination region of the transistor; and further comprising the step of:

electrically connecting the portion of the conductive material layer in the termination region to at least one of the doped semiconductor regions of the second conductivity type.

3. A method for forming a field effect transistor comprising the steps of:

providing a semiconductor substrate having a principal surface and being of a first conductivity type;

forming a patterned mask layer on the principal surface;

forming a doped deep body region of a second conductivity type of the transistor in a portion of the substrate underlying the portions of the principal surface exposed by the patterned mask layer;

locally growing oxide on the principal surface at those portions of the principal surface exposed by the patterned mask layer including on a portion of a termination region of the transistor;

removing the patterned mask layer, thereby exposing additional portions of the principal surface; and

forming in those portions of the substrate underlying the exposed additional portions of the principal surface a doped body region, a doped source region, and a gate region of the transistor.

4. A field effect transistor comprising:

a semiconductor substrate having a first conductivity type and having a principal surface;

a plurality of spaced-apart doped semiconductor regions of a second conductivity type extending from the principal surface into the substrate, being deep body regions of the transistor;

a plurality of trenches extending into the sub-

strate from the principal surface and being filled with a conductive material;

doped regions of the first and second conductivity type extending into the substrate from the principal surface adjacent at least some of the trenches, being respectively source and body regions of the transistor; and

a field oxide layer formed on portions of the principal surface, including on a portion of the principal surface at a termination region of the transistor.

5. The transistor of Claim 4, further comprising a conductive layer overlying the field oxide layer in the termination region and being in electrical contact with at least one of the doped semiconductor regions of the second conductivity type.

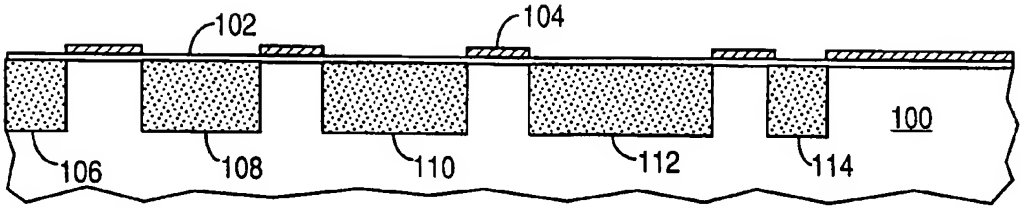

FIG. 1a

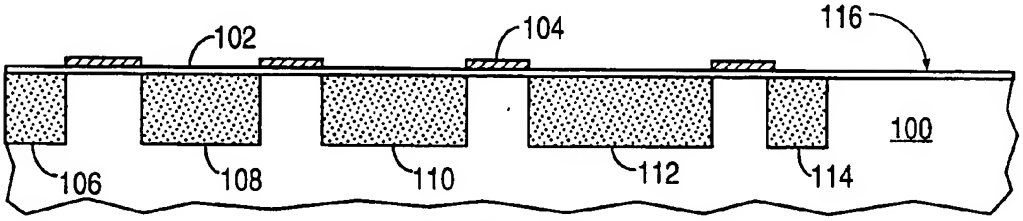

FIG. 1b

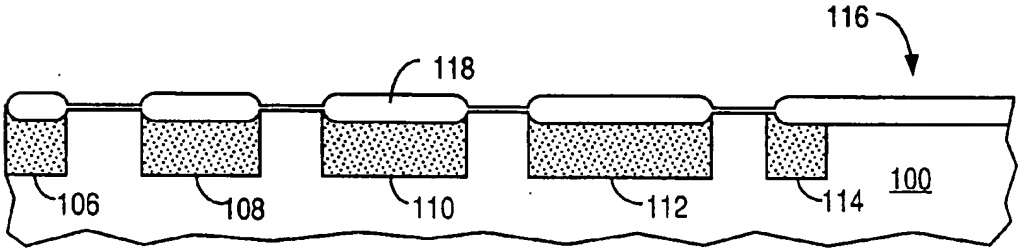

FIG. 1c

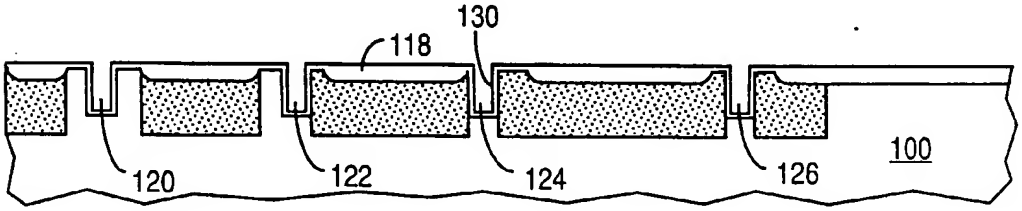

FIG. 1d

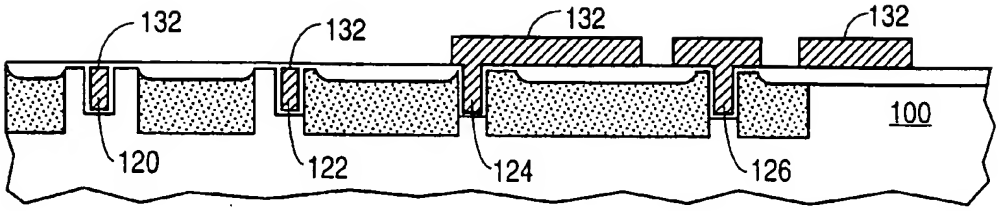

FIG. 1e

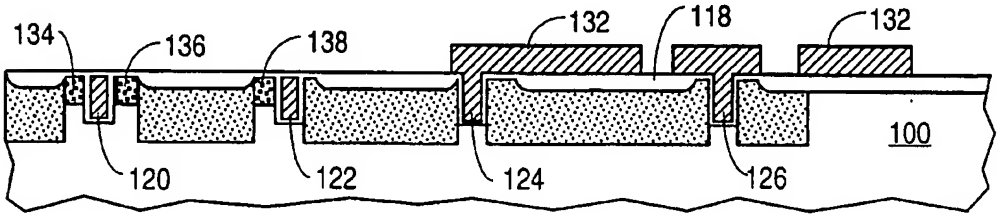

FIG. 1f

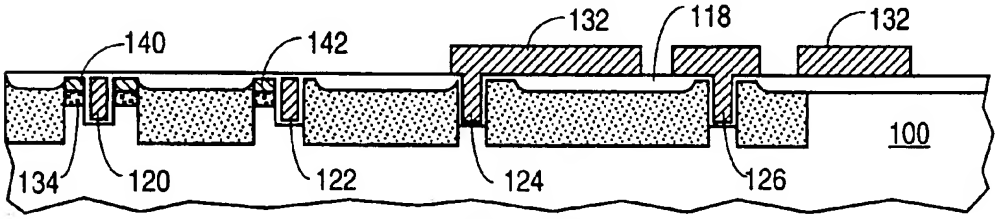

FIG. 1g

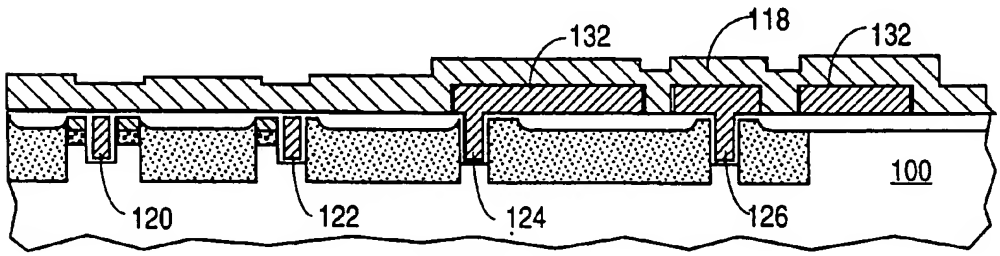

FIG. 1h

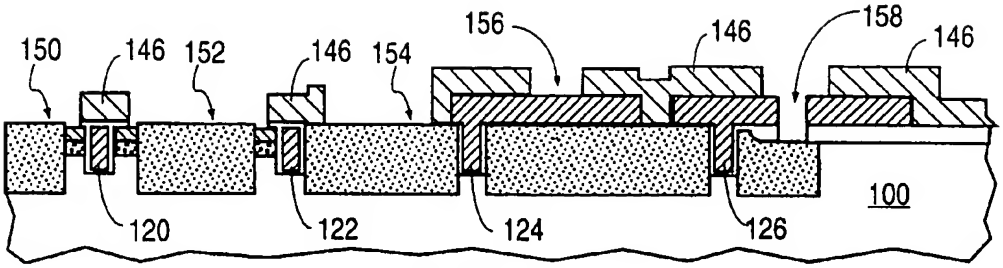

FIG. 1i

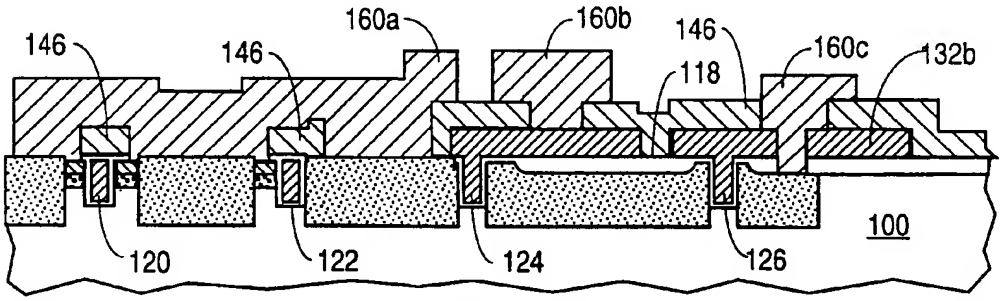

FIG. 1j

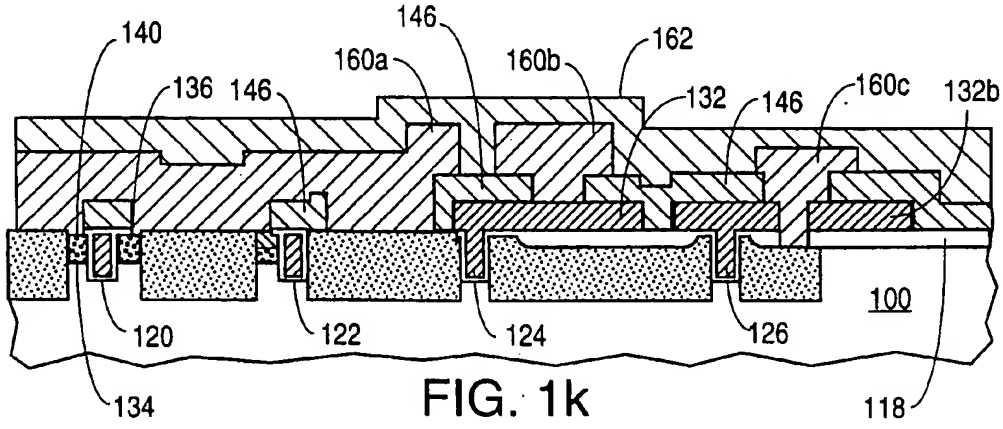

FIG. 1k